Journal of Alloys and Compounds 495 (2010) 116–120

Contents lists available at ScienceDirect

Journal of Alloys and Compounds

journal homepage: www.elsevier.com/locate/jallcom

Effect of temperature, illumination and frequency on the electrical characteristics of Cu/p-Si Schottky diode prepared by liquid phase epitaxy

A.A.M. Farag[a,*], A. Ashery[b], E.M.A. Ahmed[c], M.A. Salem[b]

[a] Thin Film Lab., Physics Department, Faculty of Education, Ain Shams University, Roxy, Cairo 11757, Egypt
[b] Physics Department, Semiconductor Lab., National Research Center (NRC) 12622, Egypt
[c] Physics Department, Solid State Lab., National Research Center (NRC) 12622, Egypt

ARTICLE INFO

Article history:
Received 19 August 2009
Received in revised form 20 January 2010
Accepted 21 January 2010
Available online 1 February 2010

Keywords:
Schottky diode
Cu/p-Si
Illumination
Frequency

ABSTRACT

Microcrystalline thin Cu films were grown by liquid phase epitaxy, LPE on p-Si substrates. At the beginning of growth some of Cu atoms firstly reacted with Si forming a silicide layer (CuSi). After which a Cu film was epitaxially grown on the silicide seeds template which plays a key role in overcoming the lattice mismatch of Cu/p-Si. The topography of the grown Cu film on Si substrates was examined by scanning electron microscopy (SEM). The structural analysis by X-ray diffraction (XRD) confirmed a formation of Cu film as well as CuSi as an intermediate step. The current–voltage (*I–V*) and capacitance–voltage (*C–V*) characteristics of metal–semiconductor (Cu/p-Si) Schottky contacts were studied in the temperature range 300–375 K. The effect of the temperature on the series resistance R_s, the ideality factor n and the barrier height Φ_b were investigated. The Cu/p-Si diode shows non-ideal *I–V* behavior with an ideality factor greater than unity that can be ascribed to the interfacial layer, the interface states and the series resistance. The *I–V* characteristics of the investigated diode under high voltage region were found to be governed by space charge-limited currents. The extracted parameters were found to be strongly temperature dependent. The photocurrent properties of the device under illumination were also investigated. The photocurrent in the reverse direction is strongly increased by photo-illumination. In addition, capacitance–voltage–frequency (*C–V–f*) characteristics were investigated at frequency range 10 kHz to 1 MHz. At each frequency, the measured capacitance decreases with increasing frequency due to a continuous distribution of the interface states.

1. Introduction

It has been well known that metal–semiconductor Schottky contacts structures have been studied extensively because of their importance in electronic and optoelectronic devices [1–3]. One of the most interesting properties of a metal–semiconductor interface is its Schottky barrier height (SBH), which is a measure of the mismatch of the energy levels for majority carriers across the metal–semiconductor interface. The SBH controls the electron transport across the metal–semiconductor interface and is vital importance to the successful operation of any semiconductor device [4–5].

During recent years, application of the surface and interface science techniques has shown clearly that interfaces formed between metals and semiconductors are complex regions whose physical properties depend on the preparation conditions of the surface. This is because in many cases, contact metals are deposited onto surfaces covered by unknown contaminants which may cause the interface states and which can affect the mechanical and electrical properties, performance, reliability and stability of metal–semiconductor (MS) devices [4–5]. Interfaces between thin metal layers and semiconductors are used in optical detector, solar cells and chemical sensors [6–8].

Cu is drawing increasing attention as an alternative to Al alloys as the metallization materials for microelectronic devices due to its low resistivity and high electromigration resistance. The interest naturally leads to concern with respect to the Cu/Si interface as well as the formation and properties of copper silicides. Peculiar feature of the Cu/Si interface is the large lattice misfit of about 15%. At the interface, silicide layer is known to be formed which plays a key role in overcoming the large lattice mismatch. On the top of the silicide interlayer, an epitaxial Cu film was grown in the layer-by-layer-like fashion [9,10].

Liquid phase epitaxy is a widely used technique in recent semiconductor technology. Good adherence of the sputter-deposited material to the substrate can be achieved for a variety of materials, metals, compound metals and oxides, making the contact to the more intimate substrate than can be obtained by other commonly used deposition techniques. The current–voltage (*I–V*) character-

* Corresponding author.
E-mail address: alaafaragg@yahoo.com (A.A.M. Farag).

0925-8388/$ – see front matter © 2010 Elsevier B.V. All rights reserved.
doi:10.1016/j.jallcom.2010.01.098

istics of the Schottky barrier diodes usually deviate from the ideal thermionic emission (TE) current model. There are currently a vast number of reports of experimental studies of characteristic parameters such as the barrier height and ideality factor in a great variety of MS contacts [11–14].

The objective of the present work is to study the structural characteristics of the Cu/p-Si Schottky diode. The temperature dependence of the current–voltage characteristics was also investigated in an attempt to obtain information about the important parameters of this diode. The photocurrent characteristics of the device were studied under white light illumination. Moreover, the capacitance–voltage–frequency measurements in the range 10 Hz to 1 MHz were applied for the characterization of this diode.

2. Experimental details

2.1. Material preparation

The liquid phase epitaxy was employed to grow layers of Cu on p-Si substrate single crystalline wafers using Indium as solvent. The multibin boat made of special graphite hardness was held in a fixed position within a silica tube. The growth temperature was controlled by means of temperature controller connected to hand-held digital thermometer with temperature prob. The system is usually evacuated to 10^{-3} torr. Prior to the growth run, purified argon is passed through the tube. The technique of LPE is described in detail elsewhere [15]. The loaded boat with p-silicon substrate single crystal with orientation (1 1 1) was used. The loaded boat was heated up to 1173 K and kept at this temperature for 30 min to homogenize the solution and then cooled down to 1123 K with a cooling rate of 1 K/min. The growth process is terminated by removing the ready substrate with its upper layer from the solution cell.

2.2. Material characterization

Scanning electron microscope, model JEOL JXA-840 A, was used to study the surface morphology of the grown Cu epilayer on p-Si single crystalline substrate. The chemical composition of the Cu/p-Si was checked by energy dispersion X-ray spectroscopy (EDS) using a scanning electron microscope (JEOL JXA-840 A). X-ray diffraction analysis was carried out using Philips X-ray diffractometer model PW 1710 with Ni filter and Co Kα radiation.

The current flowing through the sample was determined using a stabilized power supply and a high-impedance Keithley 617 electrometer. Electrical properties were performed in dark over the temperature range 300–375 K. The temperature was measured directly by means of chromel–alumel thermocouple connected to hand-held digital thermometer (Extech 421508). The incident power density of light illumination was 80 mW/cm^2 provided by a halogen tungsten lamp. The power density of illumination on the device was measured by means of a calibrated TM 20 solar power meter.

Capacitance–voltage–frequency characteristics, using HIOKI 3532 LCR Hi-TESTER in conjunction with a laboratory-made sample holder and heating arrangement with an ac signal (voltage 1.3 V) were also measured. All the above measurements were carried out within a small (±25 K) temperature interval.

3. Results and discussion

3.1. Morphology and structural characterizations

Fig. 1 shows the scanning electron micrograph of the Cu/p-Si at room temperature (300 K) describing their surface topography and microstructure. High density, crack-free and grainy surface morphology are clearly seen. The nature and distribution of microstructures suggest the accumulation of grains in some positions and then inhomogeneous distribution of Cu epilayer throughout the surface of the Si substrate.

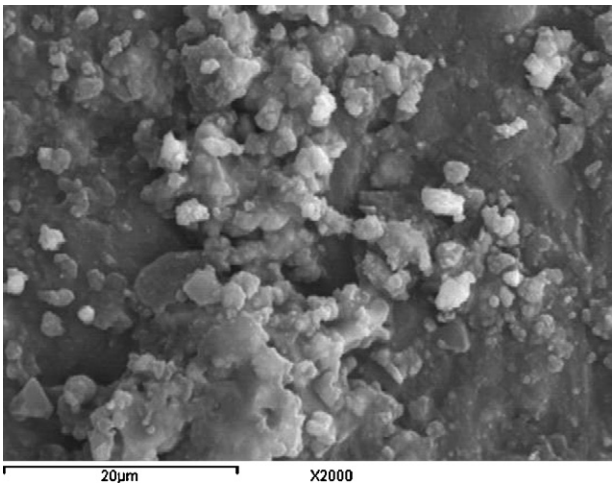

Fig. 1. Scanning electron micrograph (SEM) of Cu/p-Si device.

The crystal structure of Cu/p-Si was investigated by X-ray diffraction (XRD) technique and the results are depicted in Fig. 2. All the peaks of the XRD pattern were indexed for each reflection of the compound and seen on the pattern. All the prepared devices showed a strong peak of Si (1 1 1) orientation. There is evidence of the heteroepitaxial growth of Cu films above a Si substrate in the preferred (2 0 0) orientation. Some Cu atoms are bound to the Si at the interface between Cu/Si forming CuSi as shown for the (0 0 4) and (2 2 4) orientations. The formation of CuSi reduces the misfit between Cu and the Si substrate and then improving the properties of Cu/p-Si diodes.

3.2. Dark current–voltage characterizations

The current–voltage characteristics of a Cu/p-Si heterojunction at different temperatures in the range 300–375 K are shown in Fig. 3. The diode exhibits a rectifying effect. The current increases with increasing temperature. This suggests that the diode has a negative resistance temperature coefficient. In order to obtain quantitative information about Cu/p-Si heterojunction, both a curve fitting and theoretical analysis of our *I–V* curves have

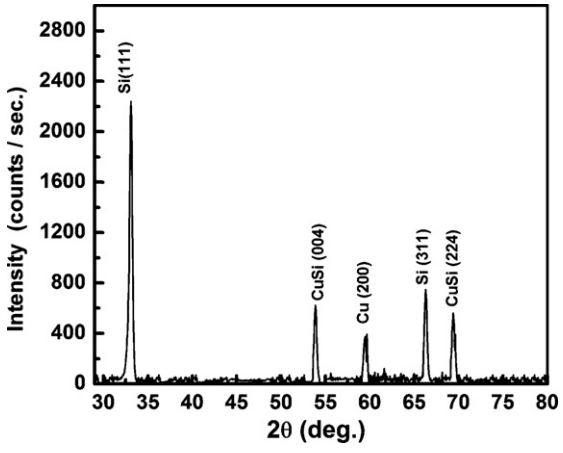

Fig. 2. XRD of Cu/p-Si device.

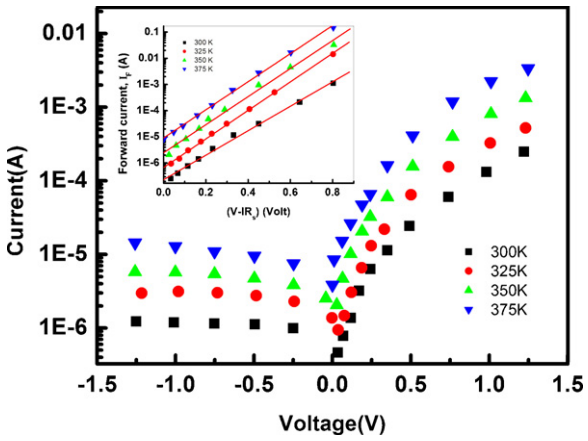

Fig. 3. Semi-logarithmic plot of both forward and reverse current vs. applied voltage at different temperatures. The inset shows Semi-logarithmic plot of forward current vs. (V–IR_s) at different temperatures.

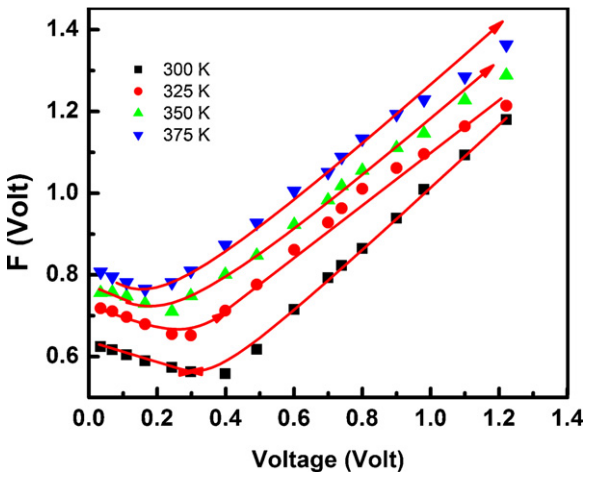

Fig. 4. Plot of $F(V)$ vs. applied voltage.

been performed. There can be distinguished two distinct regions characterize these curves indicating different conduction mechanisms, depending on the applied bias. At low voltages, there is an exponential increase in the forward current with applied voltage. This indicates the formation of the depletion region in metal/semiconductor contact.

The I–V characteristics of a Schottky barrier diode obeying the thermionic emission model are given by [16]:

$$I = AA^* \exp\left(\frac{-q\Phi_b}{kT}\right)\left[\exp\left(\frac{qV}{nkT}\right) - 1\right], \quad (1)$$

where A is the effective area of the device, A^* is the Richardson constant, n is the ideality factor and V is the applied voltage dropped on the Schottky junction. The effect of the diode resistance can be modeled with a series combination of a diode and a resistor R_s through which the current flows. The voltage V across the diode can then be expressed in term of the total voltage drop V across the series combination of the diode and the resistor. Thus, V–IR_s and for $V > 3kT/q$, Eq. (1) becomes

$$I = AA^* \exp\left(\frac{-q\Phi_b}{kT}\right)\left[\exp\left(\frac{V - IR_s}{nkT}\right)\right] \quad (2)$$

Based on this equation, the series resistance was deduced by using the method proposed by Norde that stated in [17]. The modified Norde function $F(V)$ is defined as follows:

$$F(V) = \frac{V}{2} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^*T^2}\right), \quad (3)$$

where $I(V)$ is the current obtained from the I–V curve and the other parameters are described above. Once the minimum of the $F(V)$ vs. V plot is determined, the Schottky barrier height, Φ_b can be obtained, where $F(V_o)$ is the minimum point of $F(V)$, and V_o is the corresponding voltage [18,19]. Fig. 4 shows the $F(V)$–V plots of the structure at different temperatures in the range 300–375 K. The value of the barrier height of a contact can be determined as follows (by using Norde's functions):

$$\Phi_b = F(V_o) + \frac{V_o}{2} - \frac{kT}{q}, \quad (4)$$

From the $F(V)$–V plots, some parameters of the structure (Φ_b, R_s) have been determined and listed in Table 1. The value of the series resistance was determined by following equation:

$$R_s = \frac{kT}{qI}, \quad (5)$$

where I is the current corresponds to the minimum V_o. as shown from the table that the barrier height increases with increasing temperature and the series resistance decreases slightly. When the temperature increases, more and more electrons have sufficient energy to surmount the higher barrier. Consequently, the dominant barrier height will increase with the temperature and bias voltage [20]. The decrease of R_s with the increase of temperature is believed to result due to factors responsible for increase of the ideality factor of the diode.

Theoretically, the ideality factor n of the Schottky diode made on Cu/p-Si is introduced to take into account the deviation of the experimental I–V data from the ideal thermionic emission model and can then be evaluated from the slope of a semilog plot of I vs. V–IR_s as shown in the inset of Fig. 3. However, this curve is clearly non-linear in the relatively high voltage region, indicating that another transport mechanism is present in the diode. The obtained value of the ideality factor at different temperature is listed in Table 1. The non-ideal behavior of ideality factor is commonly accounted by the existence of a thin copper silicide layer between metal and semiconductor or image force lowering of the Schottky barrier at interface [21,22].

At relatively higher voltages ($0.75 \le V \le 1.2$ V), the charge transport mechanism of the device was analyzed using $I \alpha V^m$ relation. The dominant charge transport mechanism for the device was determined by obtaining m value from the slope of linear regions in Fig. 3 after re-plotted as log I–log V (not shown). The slope was found to be larger than 2, clarifying that the forward current is space charge-limited current (SCLC) with an exponential distribution of traps. This SCLC mechanism suggests that at higher voltages, the current is limited by space charge accumulation. The SCLC mechanism by exponential distribution of traps is expressed by the following relation [23,24]:

$$I = qA\mu N_c\left(\frac{\varepsilon_s}{qN_okT}\right)^l \frac{V^{l+1}}{d^{2l+1}}, \quad (6)$$

where ε_s is the dielectric constant of the semiconductor, N_o is the trap concentration per unit energy range at the conduction band edge, d is the thickness of the semiconductor, q is the electronic charge and l is a parameter related to traps given by $l = T_t/T$, T_t is

Table 1
Parameters deduced from I–V characteristics of Cu/p-Si Schottky diode.

T (K)	Φ_b (eV)	R_s (Ω)	n	T_t (K)
300	0.73	1691	2.92	744
325	0.77	1452	2.84	726
350	0.81	1009	2.68	715
375	0.83	924	2.13	702

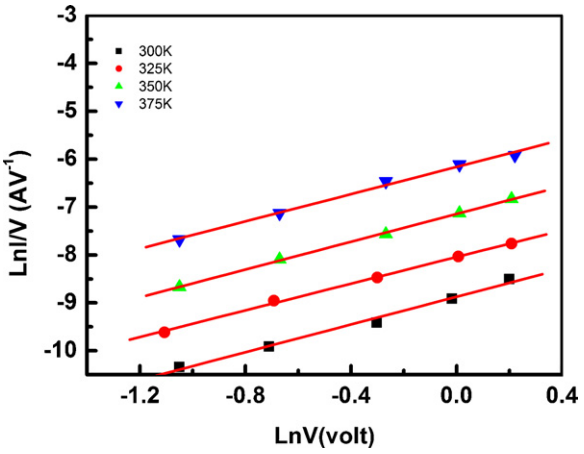

Fig. 5. Plot of ln(I/V) vs. applied voltage.

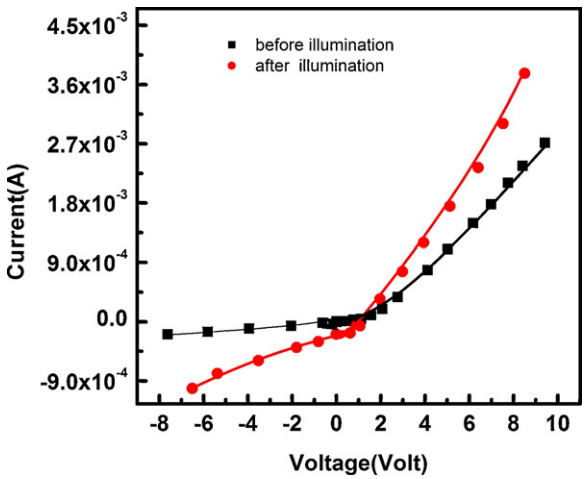

Fig. 6. Dark and illuminated I–V characteristics at room temperature.

a characteristic temperature of the exponential distribution of the traps. The obtained T_t values decrease with increasing temperature as shown in Table 1. This suggests that the total trap density decreases as the temperature increases.

3.3. Determination of state density in the Schottky diode

According to the theory of the space charge-limited current, distribution of localized states can be expressed as [25]:

$$I = KV\exp(SV), \tag{7}$$

where K is a constant and can be expressed as

$$K = \frac{qA\mu N_o}{d}, \tag{8}$$

In Eq. (7), S is the slope of ln(I/V) vs. V plot and can be given by the following form [25]:

$$S = \frac{2\varepsilon_s\varepsilon_o}{qN_{EF}\,kTd^2}, \tag{9}$$

where $N(E_F)$ is the density of localized states near the Fermi level, ε_s is the dielectric constant of the sample, ε_o is the permittivity of free space and k is the Boltzmann constant. The plots of ln(I/V) vs. V at different temperatures were plotted as shown in Fig. 5. S value was obtained from the slope of these curves. N_{EF} value was determined from the slope of S vs. 1000/T plot (not shown) and was found as $2.7 \times 10^{18}\,\mathrm{eV^{-1}\,cm^{-3}}$. It is seen that S values are proportional to the inverse of temperature. This behavior may be discussed as the temperature increases, the trapped carriers are thermally activated to the conduction band. Furthermore, interfacial layer between Cu metal and p-Si semiconductor causes a voltage drop across the interface and thus, the voltage dependence of the reverse current can be explained by the drop over an interfacial copper silicide layer.

3.4. Current–voltage characteristics under illumination

Current–voltage (I–V) characteristics of Cu/p-Si device under dark and light illumination condition of 80 mW/cm^2 are shown in Fig. 6. The increase in the photocurrent is due to the drift velocity of photogenerated electrons and holes in Si. The photocurrent in the reverse direction is strongly increased by photo-illumination. This behavior yields useful information on the electron–hole pairs which was effectively generated in the junction by incident photons. The photocurrent is higher than the dark current at the same reverse bias. This suggests that the light generates carrier-contributing photocurrent due to the production of electron–hole pairs as a result of the light absorption [25,26]. The generation of photoelectrons is due to electron transfer from Si into Cu through the potential barrier at the interface. This is a result of a difference in electron affinities between the two materials. The generated electrons are swept towards the Si along the potential barrier at the interface due to the influence of the electric field applied, whereas, holes are accelerated towards the Cu.

3.5. Capacitance–voltage–frequency characteristics

Fig. 7 shows the measured capacitance as a function of the frequency with different bias voltage of the Cu/p-Si structure at room temperature. The C–V measurements of the device have been carried out at 10, 100, 500 kHz and 1 MHz. As can be seen in Fig. 7 the measured capacitance (C) is dependent on bias voltage and frequency. Each C–V curves have three regimes of accumulation–depletion–inversion region, but with a considerable voltage-axis shift due to the presence of surface states. At high frequency, the Cu/p-Si Schottky diode with high series resistance showed decreasing capacitance with increasing frequencies. The voltage and frequency dependence is due to the particular features of Schottky barrier, impurity level, high series resistance, doping density, etc. This occurs because at lower frequencies the interface states can follow the ac signal and yield an excess capacitance, which depends on the frequency. In the high frequency limit ($f \geq 500$ kHz), the interface states cannot follow the ac signal. This makes the contribution of interface state capacitance to the total

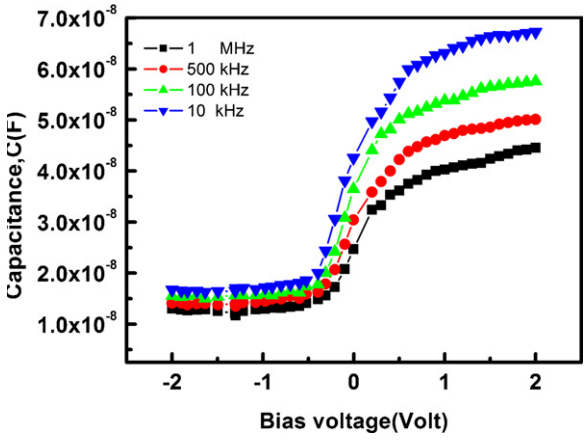

Fig. 7. The capacitance–voltage at different frequencies.

capacitance negligibly small [27,28]. From the above discussion it can be suggested that under bias voltage the interface states are responsible for the observed frequency dispersion in *C–V* curves.

4. Conclusions

The nature and distribution of microstructures checked by SEM suggested the accumulation of grains in some positions and then inhomogeneously distributed through out the surface of the material sample. The X-ray data analysis revealed a formation of CuSi interface which reduce the misfit between Cu and the Si substrate and then improving the properties of Cu/p-Si heterojunctions. The *I–V* characteristics have shown that the diodes exhibit rectifying properties. The data analysis revealed an increase in the zero bias barrier height and decrease in the ideality factor with temperature increasing. The photovoltaic properties were investigated through *I–V* measurements. Photovoltaic measurements indicated that Cu/p-Si Schottky diodes have sensitive to the light, proposing a good candidate as a photodiode. The capacitance–voltage–frequency (*C–V–f*) measurements of Cu/p-Si Schottky diodes confirmed that the interface states can follow the ac signal and yield an excess capacitance at low frequencies.

References

[1] G. Güler, Ş. Karataş, Ö. Güllü, Ö.F. Bakkaloğlu, J. Alloys Compd. 486 (2009) 343–347.
[2] V. Baranwal, S. Kumar, A.C. Pandey, D. Kanjilal, J. Alloys Compd. 480 (2009) 962–965.
[3] A.A.M. Farag, I.S. Yahia, M. Fadel, Int. J. Hydrogen Energy 34 (2009) 4906–4913.
[4] V. Janardhanam, A. Ashok Kumar, V. Rajagopal Reddy, P. Narasimha Reddy, J. Alloys Compd. 485 (2009) 467–472.
[5] H. Altuntaş, Ş. Altındal, S. Özçelik, H. Shtrikman, Vacuum 83 (2009) 1060–1065.
[6] N. Yıldırım, A. Türüt, Microelectron. Eng. 86 (2009) 2270–2274.
[7] K. Ejderha, N. Yıldırım, A. Türüt, B. Abay, Superlattice Microstruct. 47 (2010) 241–252.
[8] H. Korkut, N. Yıldırım, A. Turut, Physica B 404 (2009) 4039–4044.
[9] Kurt W. Kolasinski, Handb. Surf. Sci. 3 (2008) 787–870.
[10] X. Tang, H. Zhanga, H. Sua, Z. Zhonga, Y. Jinga, Physica E 40 (2008) 3004–3008.
[11] T. Tanaka, M. Tanaka, M. Itakura, T. Sadoh, M. Miyao, Thin Solid Films 518 (2010) S170–S173.
[12] S. Hayashi, M. Nangu, T. Morikuni, S. Owa, N.S. Takahashi, J. Cryst. Growth 311 (2009) 842–846.
[13] J. Kobayashi, N. Ohashi, H. Sekiwa, I. Sakaguchi, M. Miyamoto, Y. Wada, Y. Adachi, K. Matsumoto, H. Haneda, J. Cryst. Growth 311 (2009) 4408–4413.
[14] S. Sommadossi, L. Litynska, P. Zieba, W. Gust, E.J. Mittemeijer, Mater. Chem. Phys. 81 (2003) 566–568.
[15] A.A.M. Farag, A. Ashery, F.S. Terra, Microelectron. J. 39 (2008) 253–260.
[16] A. Tataroğlu, Ş. Altındal, J. Alloys Compd. 479 (2009) 893–897.
[17] Ş. Karataş, Ş. Altındal, A. Türüt, M. Çakar, Physica B 392 (2007) 43–50.
[18] Y.S. Ocak, T. Kılıçoğlu, G. Topal, M.H. Başkan, Equipment 612 (2010) 360–366.
[19] G. Güler, Ş. Karataş, Ö.F. Bakkaloglu, Physica B 404 (2009) 1494–1497.
[20] Ş. Aydoğan, M. Sağlam, A. Türüt, Y. Onganer, Mater. Sci. Eng. C-Biol. Sci. 29 (2009) 1486–1490.
[21] İ. Yücedağ, Ş. Altındal, A. Tataroğlu, Microelectron. Eng. 84 (2007) 180–186.
[22] R. Şahingöz, H. Kanbur, M. Voigt, C. Soykan, Synthetic Met. 158 (2008) 27–731.
[23] Ö. Güllü, Ş. Aydoğan, A. Türüt, Microelectron. Eng. 85 (2008) 1647–1651.
[24] M. Şahin, H. Durmuş, R. Kaplan, Appl. Surf. Sci. 252 (2006) 6269–6274.
[25] F. Yakuphanoglu, S. Nihat Tugluoglu, Karadeniz, Physica B 392 (2007) 188–191.
[26] F. Yakuphanoglu, Physica B 388 (2007) 226–229.
[27] S. Karatas, A. Turut, Vacuum 74 (1) (2004) 45–53.
[28] B. Akkal, Z. Benamara, B. Gruzza, L. Bideux, Vacuum 57 (2000) 219–228.